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HITT GAINES, PC
LSI Corporation
PO BOX 832570
RICHARDSON, TX 75083

EXAMINER	
PUENTE, EVA YI ZHENG	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@hittgaines.com

ND

Office Action Summary	**Application No.** 10/685,018	**Applicant(s)** SUN ET AL.	
	Examiner Eva Yi Zheng	**Art Unit** 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 8/17/07.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 8/17/07 have been fully considered but they are not persuasive. Examiner has thoroughly reviewed Applicant's arguments but firmly believes that the cited reference reasonably and properly meet the claimed limitation as rejected.

Applicant's argument – (1) Prior art Yamamoto (US 5,991,350) does not teach or suggest providing a second signal based on comparing first and second samples of a comparison signal when the comparison signal is below a threshold level as recited in independent claims 1 and 8. (2) Yamaoto does not suggest using a comparing signal to either fine tune or reset a phase shift. (3) Applicant find no where in Matsuoka to cure the deficiencies of Yamamoto in rejections made to claims 4,6,7,11,13 and 14 under 35 U.S.C. 103(a). (4) Applicant find no where in Adachi to cure the deficiencies of Yamamoto in rejections made to claim 15 under 35 U.S.C. 103(a). (5) Applicant find no where in Matsuoka to cure the deficiencies of Yamamoto and Adachi in rejections made to claim 18,20 and 21 under 35 U.S.C. 103(a).

Examiner's response – (1) It appears that applicant misunderstood Examiner's position over rejections. Yamamoto disclose a PLL circuit that comprise a phase comparator (101 in Fig. 1) to receive a signal from source and a comparison signal; and generate logic H/ logic L signals based on first and second samples of the comparison signal ($S_{pD1(t)}$ and $S_{pD1(t-1)}$; POLARITY S_p and 203 in Fig. 2) with the condition when the comparison signal is below a threshold level (H: $S_{pD1} \leq \delta$ in Fig. 2). When the $S_{pD1(t)}$

value is less than/below to a threshold value (δ), the selector (202 in Fig. 2) will select SpD4. On the other hand, when the condition of SpD1(t) value is greater than the threshold value (δ), the selector will select signal SpD3. Even when SpD1(t) and SpD1(t-1) values are continuously compared, it produces meaningless information if the condition of below threshold is not meet in the selector (Col 4, L19-53). Yamamoto meet the claimed limitations. (2) There are no such limitations in claims citing to fine tune or reset a phase shift. Therefore, Yamamoto meet the claimed limitations. (3) Matsuoka et al make up the deficiencies by disclose a phase synchronization system comprising a phase comparator, a counter control, and a judgment section (Fig. 4), wherein the counter controller controls the counter number to increment, decrement, or left unchanged depends on the signal conditions. The judgment section generates a reset signal to counter if the threshold is reached (Fig. 5; Col 10, L31-L46). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of counter controller and error judgment by Matsuoka et al in the phase locked loop teaching of Yamamoto. By doing so, provide high degree of phase synchronization accuracy in a communication system. (4) Yamamoto discloses all the subject matters except for the specific teaching of components in the transmitter. However, Adachi et al, disclose a transmitter system comprises input I and Q signals (1 and 2 in Fig. 4), a power amplifier (5 and 6 in Fig. 4), and a digitally controlled phase shifter (19 Fig. 4). A phase shifter is feedback to the input for phase error correction (Col 1, L34 - Col 3, L13). It is well known that a digital control oscillator generates in-phase and quadrature signals. Therefore, it is obvious to one of ordinary skill in art to implement the teaching of I and Q signals, power amplifier and phase shifter by Adachi et al in the PLL circuit of Yamamoto. By doing so, increase data rate and provide high degree of phase synchronization accuracy in a communication system. (5) Yamamoto disclose all the subject matters except for the specific teaching of adder/decoder is configured to maintain the current number, to provide a rest signal and reset number empirically. However, Matsuoka et al disclose a phase synchronization system comprising a phase comparator, a counter control, and a judgment section (Fig. 4), wherein the counter controller controls the counter number to increment, decrement, or left unchanged depends on the signal conditions. The judgment section generates a reset signal to counter if the threshold is reached (Fig. 5; Col 10, L31-L46). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of counter controller and error judgment by Matsuoka et al in the phase locked loop teaching of Yamamoto. By doing so, provide high degree of phase synchronization accuracy in a communication system.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5, 8-10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US 5,991,350).

a) Regarding to claims 1 and 8, Yamamoto disclose an adaptive phase controller employing a threshold level, comprising:

a comparator configured to receive a comparison signal representing a phase (101 in Fig. 1) and to provide a second signal (H and L signals in Fig. 2) based on comparing first and second samples of said comparison signal ($S_{pD1(t)}$ and $S_{pD1(t-1)}$) when said comparison signal is below said threshold level (107 in Fig. 1); and

an adder/decoder coupled to said comparator and configured to adjust a current number corresponding to said phase based on said second signal (203 in Fig. 2; Col 4, L19-35).

Yamamoto teaches a phase locked loop circuit generates a phase comparison signal and adjust the signal with H or L based upon the condition when the $S_{pD1(t)}$ value is less than/below to a threshold value. The selector will select S_{pD4}. In other words, when the condition of $S_{pD1(t)}$ value is greater than the threshold value, the selector will select signal S_{pD3}. Even when $S_{pD1(t)}$ and $S_{pD1(t-1)}$ values are continuously compared, it produces meaningless information if the condition of below threshold is not meet in the selector (Fig. 2). Although Yamamoto did not disclose the specific order of comparison for threshold value, then comparing the first and second samples, Yamamoto and current application only differ in processing steps and do not alter end results. They both produce phase control signals in various conditions, especially when the signal is below the threshold value. Also, current application did not disclose any specific reason or advantage to perform phase control in such way as claimed.

Therefore, it is obvious to one of ordinary skill in art to recognize that Yamamoto is functional equivalent and produce the same results as the current application.

b) Regarding to claims 2 and 9, Yamamoto disclose when said adder/decoder is configured to increment said current number when said first sample is great than said second sample (n-bit addition 203 in Fig. 2)

c) Regarding to claims 3 and 10, Yamamoto disclose when said adder/decoder is configured to decrement said current number when said first sample is less than said second sample (n-bit subtraction 203 in Fig. 2).

d) Regarding to claims 5 and 12, Yamamoto disclose wherein said comparator is further configured to provide a reset signal when said comparison signal reaches said threshold level (output of 101 and start/reset in Fig. 1)

4. Claims 4, 6, 7, 11, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US 5,991,350) in view of Matsuoka et al (US 5,463,627).

a) Regarding to claims 4, 6, 7, 11, 13 and 14, Yamamoto disclose all the subject matters above except for the specific teaching of adder/decoder is configured to maintain the current number, to provide a rest signal and reset number empirically.

However, Matsuoka et al disclose a phase synchronization system comprising a phase comparator, a counter control, and a judgment section (Fig. 4), wherein the counter controller controls the counter number to increment, decrement, or left unchanged depends on the signal conditions. The judgment section generates a reset signal to counter if the threshold is reached (Fig. 5; Col 10, L31-L46).

Therefore, it is obvious to one of ordinary skill in art to combine the teaching of counter controller and error judgment by Matsuoka et al in the phase locked loop teaching of Yamamoto. By doing so, provide high degree of phase synchronization accuracy in a communication system.

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US 5,991,350) and in view of Adachi et al (US 5,802,451).

a) Regarding to claim 15, Yamamoto disclose an adaptive phase controller, comprising:

an input section that receives phase input and feedback signals and provides phase output signals (101 in Fig. 1);

a feedback section that provides phase feedback signals to said input section (output of VCO 105 in Fig.1);

a local oscillator section that is coupled to said feedback section (VCO 105 in Fig.1);

a comparator configured to receive a comparison signal representing a phase (101 in Fig. 1) and to provide a second signal (H and L signals in Fig. 2) based on comparing first and second samples of said comparison signal ($S_{pD1(t)}$ and $S_{pD1(t-1)}$) when said comparison signal is blow said threshold level (107 in Fig. 1); and

an adder/decoder coupled to said comparator and configured to adjust a current number corresponding to said phase based on said second signal (203 in Fig. 2; Col 4, L19-35).

Yamamoto teaches a phase locked loop circuit generates a phase comparison signal and adjust the signal with H or L based upon the condition when the SpD1(t) value is less than or below to a threshold value. The selector will select SpD4. In other words, when the condition of SpD1(t) value is greater than the threshold value, the selector will select signal SpD3. Even when SpD1(t) and SpD1(t-1) values are continuously compared, it produces meaningless information if the condition of below threshold is not meet in the selector (Fig. 2). Although Yamamoto did not disclose the specific order of comparison for threshold value, then comparing the first and second samples, Yamamoto and current application only differ in processing steps and do not alter end results. They both produce phase control signals in various conditions, especially when the signal is below the threshold value. Also, current application did not disclose any specific reason or advantage to perform phase control in such way as claimed. Therefore, it is obvious to one of ordinary skill in art to recognize that Yamamoto is functional equivalent and produce the same results as the current application.

Yamamoto discloses all the subject matters above except for the specific teaching of other components in the transmitter.

However, Adachi et al, disclose a transmitter system comprises input I and Q signals (1 and 2 in Fig. 4), a power amplifier (5 and 6 in Fig. 4), and a digitally controlled phase shifter (19 Fig. 4). A phase shifter is feedback to the input for phase error correction (Col 1, L34 - Col 3, L13). It is well known that a digital control oscillator generates in-phase and quadrature signals. Therefore, it is obvious to one of ordinary skill in art to implement the teaching of I and Q signals, power amplifier and phase shifter by Adachi et al in the PLL circuit of Yamamoto. By doing so, increase data rate and provide high degree of phase synchronization accuracy in a communication system.

b) Regarding to claim 16, Yamamoto disclose when said adder/decoder is configured to increment said current number when said first sample is great than said second sample (n-bit addition 203 in Fig. 2)

c) Regarding to claim 17, Yamamoto disclose when said adder/decoder is configured to decrement said current number when said first sample is less than said second sample (n-bit subtraction 203 in Fig. 2).

d) Regarding to claim 19, Yamamoto disclose wherein said comparator is further configured to provide a reset signal when said comparison signal reaches said threshold level (output of 101 and start/reset in Fig. 1)

6. Claims 18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US 5,991,350), in view of Adachi et al (US 5,802,451), and further in view of Matsuoka et al (US 5,463,627).

a) Regarding to claims 18, 20 and 21, Yamamoto disclose all the subject matters above except for the specific teaching of adder/decoder is configured to maintain the current number, to provide a rest signal and reset number empirically.

However, Matsuoka et al disclose a phase synchronization system comprising a phase comparator, a counter control, and a judgment section (Fig. 4), wherein the counter controller controls the counter number to increment, decrement, or left unchanged depends on the signal conditions. The judgment section generates a reset signal to counter if the threshold is reached (Fig. 5; Col 10, L31-L46).

Therefore, it is obvious to one of ordinary skill in art to combine the teaching of counter controller and error judgment by Matsuoka et al in the phase locked loop teaching of Yamamoto. By doing so, provide high degree of phase synchronization accuracy in a communication system.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Y Zheng whose telephone number is 571-272-3049. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eva Yi Zheng
Examiner
Art Unit 2611

October 15, 2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER